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Integration of Organic-Electrochemical Transistors into Composite Material for Structural Health Monitoring

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Abstract

Monitoring the structural health of composite materials such as fiber-laminates is essential for the safe use of these materials e.g. in the aviation or building sector. Thin and flexible sensors as well as signal processing circuits based on organic-electrochemical transistors (OECTs) can potentially be embedded into composite materials, providing a means of sensing and data processing inside the material, which can be used to monitor for potential damage. In the current work, OECTs are investigated for their potential to be integrated into composite panels. Specifically, we investigate the stability of OECTs inside fiber laminates and the influence of processing conditions (temperature, pressure) on the device performance. During processing of composite plates, the devices will be exposed to high temperatures and high pressures, which can lead to a change in the properties of the OECTs, potentially damaging the devices. Besides investigating the integration and technological challenges, simulation of OECT devices using Verilog-A models and the Spice3 simulator as well as a composition of a small signal processing circuit are studied. The parametrizable simulation model is fitted to experimental OECT output curves. The goal is to integrate the entire information and communication technology in analog electronics providing advantages in power consumption and component density compared to digital and microcontroller circuits commonly used in sensor nodes. We investigate the behavior of real devices as well as electronic simulation using Verilog-A device models based on physical models and experimental data. A simple OECT difference amplifier circuit is analyzed. In this work we outline the roadmap to fully integrated smart sensors and sensor networks using additive technologies and in-sensor analog signal and information processing.

Keywords: OECT; SHM; FRP; embedded computing; smart; sensor; network; in-sensor signal processing

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1. Introduction

Fiber-reinforced composites (FRP) are known to offer an excellent combination of high strength and stiffness with low weight, and are therefore used in more and more applications. However, barely visible impact damage as well as invisible fiber breakages can lead to early failure and premature end of life. Monitoring the structural health of FRPs is essential for a safe and long use of these materials, especially in applications that face heavy loads and higher fatigue potential, like aviation or construction.

Material-integrated sensors can help to implement structural health monitoring (SHM) systems. Often, research is focused on the sensor itself, in particular when it is integrated into FRPs, and it is tried to keep the sensor as thin as possible [5, 15, 13, 14]. Also, adding holes to the substrate to allow for improved resin flow during FRP manufacturing is a well-known strategy to achieve structurally compatible sensor integration [9]. On the other hand, sensors have to be attached to either an interface for external data processing or to a material-integrated sensor node. These sensor nodes are often bulky when using commercial components due to limitations by the available component packages soldered to printed circuit boards, even if the latter are as thin and flexible as available.

An alternative can be found in organic electronics, e.g. organic-electrochemical transistors (OECTs). These inherently thin and flexible devices can be modified to work as sensors [19, 12], as well as complementary logic circuits [18, 8, 7, 11]. OECTs can be embedded between the layers of the laminate, providing a possibility to detect changes in the material early on while minimizing the weakening of the mechanical integrity of the material.

OECTs consist of a mixed organic conductor, whose conductivity can be controlled by the injection of ions from an electrolyte into the channel. OECTs are currently tested for their use in the field of bio-electronics, making use of their bio-compatibility and low operating voltages [12]. However, due to their flexibility and thin structure, OECTs can potentially be integrated into composite materials as well, providing a means of sensing and data processing inside the material that can be used to monitor for potential damage. This is especially interesting for plate-like structures built of composite prepreg, since an integration between the prepreg layers would be possible.

In order to investigate the suitability of implementing such material-integrated data processing using OECTs, the effects of the embedding process are investigated in detail. For this, the OECTs are exposed to high temperatures separately before they are finally integrated into the material, while changes in the OECT transfer behavior are evaluated. Additionally, the electronic modeling required for circuit development is investigated. The aim is a parameterizable Verilog-A model that can be used for circuit simulation, e.g., by using the *ngspice* simulator software [20]. This model should provide the following features:

1. Output characteristics close to real components (small reality gap);
2. Characteristics based on geometrical and physical parameters, e.g., channel width;
3. Inclusion of environmental parameters, e.g., temperature, strain, pressure;
4. History, i.e., a state-base model, to account for hysteresis and altering effects.

In this work we investigate preliminary simplified models, actually not covering device history and environmental parameters like temperature or mechanical stress and their impact on the device behavior and transfer curves. But, we show the principles to derive a simulation model and its constraints, finally used in an electronic simulation of a single-stage OECT difference amplifier.

The aim of this study is to determine the challenges and limits of OECT material integration for monitoring purposes, a simulative validation for using OECTs for signal processing as well as to identify the most important areas for improvement to successfully use OECTs for this purpose in the future.

2. Materials and Methods

2.1. Flexible OECTs

The OECTs are fabricated similarly to the process presented by Frulani et al. [2], but adjusted for material integration. In particular, the samples are peeled from the rigid silicon wafer as last step to get fully flexible devices.

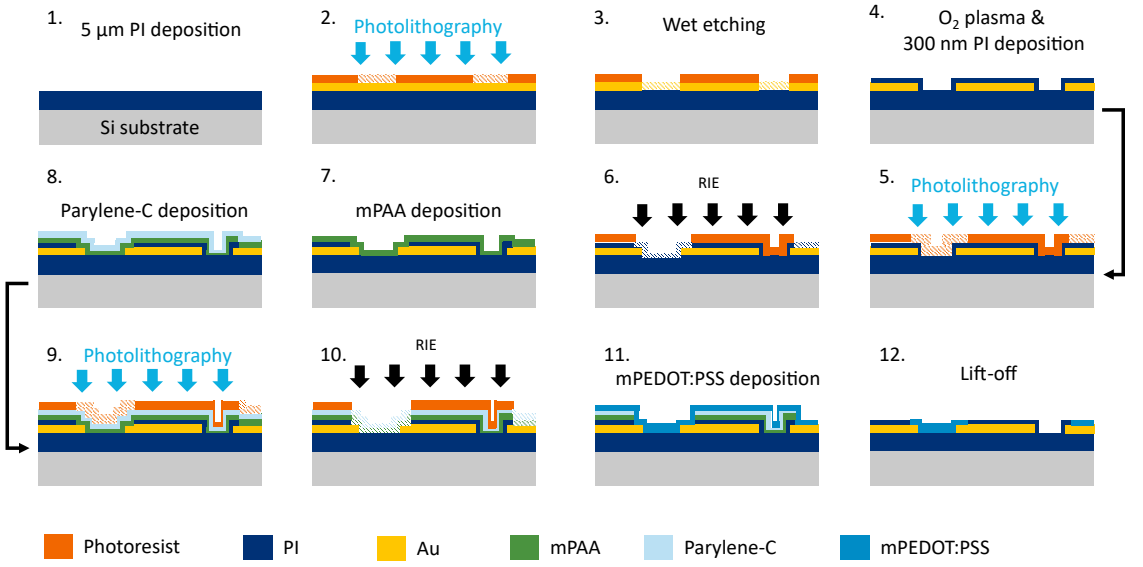


Fig. 1. Schematic process steps of flexible OECTs from step 1-10, simplified without sputtering, oxygen plasma, and removal of photoresist. 1.) Spin-coating of 5 µm Poylimide (PI) layer. 2) Sputtering of 200 nm gold (Au) and photolithography steps. 3.) Wet-chemical etching of Au. 4.) Spin-coating of 300 nm PI. 5.) Photolithography steps. 6.) Reactive ion etching (RIE) of PI - etching free pads and sensor outline. 7.) Spin-coating of mixed poly(acrylic acid) (mPAA). 8.) Deposition of parylene-C. 9.) Photolithography steps. 10.) RIE of parylene, mPAA and PI on gate, channels, pads and outline. 11.) Spin-coating of mPEDOT:PSS. 12.) Lift-off by dissolving mPAA in water.

Furthermore, perforations are added in the flexible substrate to allow for better resin flow and adhesion during the embedding process.

The fabrication steps are depicted in Fig. 1. On a 101.6 mm (4-inch) silicon wafer, a 5 µm thick polyimide layer (PI) (U-Varnish S, UBE Corp.) is spin-coated and cured under vacuum as a starting layer without adhesion promoter to enable device peeling for flexible OECTs at the end of all process steps. After that, 200 nm gold is sputtered on top using magnetron DC sputtering (Pro Line PVD 75, Kurt J. Lesker Company Ltd.), after which photolithography (AZ 1518, MicroChemicals GmbH), and wet chemical etching (Auetch 200, NB Technologies GmbH) steps are executed to create the connection tracks, drain-, source-, and gate-electrodes. To improve the adhesion of the next 300 nm thick PI layer (diluted PI in N-Methyl-2-pyrrolidone (NMP - Sigma-Aldrich); ratio 1:1) for electrical insulation, an oxygen plasma treatment (STS ICP) of 30 s is applied. After structuring the second PI layer in the pad- and transistor outline-region, a sacrificial layer of mixed poly(acrylic acid) (mPAA) mix is required. The mPAA is mixed from 1 mL of PAA solution with 3.25 mL of saturated NaOH solution to achieve a pH scale of 7.5. After that de-ionized (DI) water is added in a 1:9 ratio to achieve a 2.5 % aqueous solution of PAA. The mPAA solution is then spin-coated (4000 rpm, 25 s) and dried at 100 °C for 120 s, to be covered with a 2 µm thick parylene-C layer using a Labcoater series 300 (Plasma Parylene Systems GmbH, Rosenheim, Germany). After this, parylene, mPAA, and the 300 nm PI layer are etched using oxygen plasma (STS ICP) for 9 min to open the channel, pad, and gate regions as well as the outline of the transistors. After this, mPEDOT:PSS is prepared by mixing PEDOT:PSS (Clevios PH 1000, Heraeus) with 5 % vol. Ethylene glycol (EG), 0.1 % vol. 4-dodecylbenzenesulfonic acid (DBSA) and 1 % vol. (3-glycidyloxypropyl)trimethoxysilane (GOPTS) (EG, DBSA and GOPTS purchased from Sigma-Aldrich), sonicating the mixture for 15 min and depositing it on the wafer through a 0.45 µm pore size PTFE filter (Merck Millipore). The mPEDOT:PSS is then spin-coated (1000 rpm, 60 s) and dried on a hotplate at 110 °C for 10 min. The wafer is then immersed in DI water for a duration ≥ 12 h for the final structuring by lift-off due to the water-soluble mPAA layer.

2.2. *Electrolyte*

The choice for the electrolyte is limited by the fact that during the embedding process at elevated temperatures (≫ 100 °C) liquid electrolytes are unsuitable. We recently showed that ionic liquid crystal elastomers (iLCE) are promising solid electrolytes for OECTs [1].

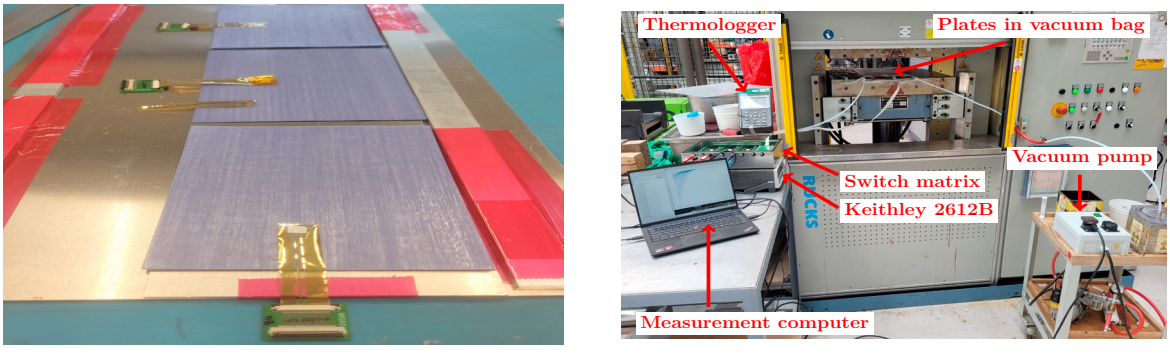
Therefore, an iLCE in the isotropic configuration, yielding faster transient response and lower hysteresis compared to the other configurations, will be used for the presented experiments.

2.3. FRP plate manufacturing

The FRP plates were produced with the Glass Fiber Prepreg FM94-27%-S-2GLASS-187-460. According to the datasheet [10], the material should be processed in an autoclave at a temperature of 120 °C and a pressure of 0.28 MPa. Since no autoclave was available for the experiments, a hydraulic press with hot plates (Rucks KV 214) and a vacuum bag was used to simulate the manufacturing process with an autoclave.

In a first step, two aluminum beams of the same size were mounted on an aluminum plate. These beams ensure that the pressure is applied homogeneously, even if the press plunger is not initially placed flat on the object, as the beams align the plunger. In total, three 150 × 100 mm plates with 16 prepreg layers each were produced. The plates were placed at the aluminum plate between the beams by stacking prepreg sheets on top of each other where the OECTs were embedded exactly in the center between the 8th and 9th layer; see Fig. 2 (a). After the stacking was complete, the stacked layers extended over the aluminum beams to ensure that the presses applied the pressure to the FRP plates. To be able to measure the temperature actually applied to the specimens, a temperature sensor was placed close to the prepreg stacks. Then another aluminum plate was placed on top of the structure; the entire setup was then placed in a vacuum bag, with all the cables required for the measurements routed airtight to the outside. The vacuum bag was then placed into the hot press, where a vacuum pump was attached to the vacuum bag. The vacuum pump was then used to create a vacuum that remained constantly below the maximum permitted pressure of 0.081 MPa [10]. The cables of the OECT and temperature sensor were connected to the switch matrix, again connected to a 2-channel source measurement unit (Keithley 2612B, Tektronix) and thermologger, respectively. A photo of the setup can be seen in Fig. 2 (b).

At the press, a pressure of 6 bar was set; due to the combined area of the three stacks, this pressure corresponds to an effective pressure of approx. 4.2 bar applied to each stack, which is more than the required 2.8 bar. This pressure was held till the end of the plate production. After the pressure was applied, the heating process was started. At the press, a temperature of 125 °C was set. During the heating phase, the temperature was increased by 3 °C/min. Also the transfer curves of one of the OECTs were measured during this phase. After 125 °C was reached, the temperature was held over 90 min. However, it should be mentioned that the 125 °C degrees were measured with the sensor of the press, but the temperature sensor that was placed at the FRP plates only measured a temperature of 95 °C degrees. After the 90 min, the press started with water cooling, and after a temperature of 40 °C was reached, the pressure was also released. Finally, the plates were demolded.



(a) (b)

Fig. 2. Pictures of the OECT embedding process. (a) Stacks of prepreg with the OECT placed at the middle layer. (b) Plates in a vacuum back placed in the hot press, with measurement devices.

2.4. Measurement setup

For OECT measurements, a setup consisting of a switch matrix, which allows for an automated switching between the ten transistors on one substrate, followed by a 2-channel source measurement unit (Keithley 2612B, Tektronix) was used, both controlled by the software SweepMe! (sweep-me.net). All measurements were performed at a drain-source voltage V_{ds}=−0.5 V and with the gate-source voltage V_{gs} varying at a low speed by 0.05 V every 1.5 s to account for the expected hysteresis well known for solid electrolytes compared to liquid electrolytes [21].

2.5. Electronic simulation and electronic modeling

There are different models available for the electronic modeling of OECT devices. They differ in accuracy and parameterization [3]. Such models can be classified in:

1. Physical models used for the description and evaluation of the device characteristics and deeper understanding of ion flows;
2. Surrogate models that are used in electronic simulation for circuit design and test.

The first class uses such models commonly in specific parameter ranges including input and output currents and voltages, i.e., in the interpolation range, whereas the second model class is used by a electrical circuit solver or, e.g., by a Machine Learning trainer supporting analog Artificial Neural Networks. The second approach cannot guarantee that the model is used in its intended parameter space, interpolation as well as extrapolation can occur, which can be have a significant impact on the use-case. We have two design goals for these models:

1. Accuracy and precision with respect to real devices;
2. ”Smooth” model behavior in the extrapolation space, i.e., avoiding steep gradients, divergence, or oscillation outside of the intended parameter space.

This work investigates primarily the impact of device integration into materials on the device characteristics and transfer curves. Therefore, the physical as well electronic models have to be sensitive and parameterizable to environmental parameters, at least to temperature. In contrast to temperature effects, which can be easily modeled, implementing mechanical effects is more complex. The electronic model introduced in Sec. 2.5.1 will actually not consider environmental effects and should be considered as a starting point for electronic simulation.

2.5.1. Electronic model

The electronic model describes the drain current I_d in dependence of the drain-source voltage V_{ds} and the gate-source voltage V_{gs} and is based on a standard OECT model [3]. The mathematical model is split in different quadrants depending on the polarity of V_{ds} and the relation of V_{gs} to V_{ds} or V_{dsat}, which is the difference of V_{gs} and the pinch-off voltage V_p:

$$V_{dsat} = V_{gs} - V_p$$

$$I_d = \begin{cases} \begin{cases} G \cdot \left(1 - \frac{V_{gs} - 0.5 \cdot V_{ds}}{V_p}\right) \cdot V_{ds} \ , \ V_{ds} \leq V_{gs} \\ G \cdot \left(V_{ds} - \frac{V_{gs}^2}{2 \cdot V_p}\right) \quad , \ V_{ds} > V_{gs} \end{cases} & , \ V_{ds} > 0 \\ \begin{cases} -\frac{G \cdot V_{dsat} \cdot V_{dsat}}{2 \cdot V_p} & , \ V_{ds} \leq V_{dsat} \\ G \cdot \left(1 - \frac{V_{gs} - 0.5 \cdot V_{ds}}{V_p}\right) \cdot V_{ds} \ , \ V_{ds} > V_{dsat} \end{cases} & , \ V_{ds} \leq 0 \end{cases} \tag{1}$$

The functional-equivalent Verilog-A model is shown in Def. 1. The model is converted into an OSDI model using the *openvaf* tool, which can be finally imported by *ngspice*. The model can be parameterized by the channel conductance G and pinch-off voltage V_p to fit the model to real devices.

Def. 1. Simple four-quadrant quadratic Verilog-A OECT $I_d(V_{gs},V_{ds})$ model using experimentally determined conductance G and pinch-off voltage V_p.

```
module oect(g,d,s);
inout g,d,s;
electrical g,d,s;
parameter real G=2.6e-3;      // Channel conductance (S)
parameter real Vp=0.7;     // Pinch-off voltage (V)
real Vgs,Vds,Vdsat,Ids;
analog begin
  Vgs=V(g,s);
  Vds=V(d,s);
  Vdsat=Vgs-Vp;
  //REGION CURRENTS//
  if (Vds > 0) begin
    if (Vds<=Vgs) begin
      Ids=G*(1-(Vgs-0.5*Vds)/Vp)*Vds;
    end else begin
      Ids=G*(Vds-pow(Vgs,2)/(2*Vp));
    end
  end else begin
    if (Vds<=Vdsat) begin
      Ids=-(G*Vdsat*Vdsat)/(2*Vp);
    end else begin
      Ids=G*(1-(Vgs-0.5*Vds)/Vp)*Vds;
    end
  end
  I(d,s)<+Ids;
end
endmodule
// model usage in SPICE
.model oect oect G=0.0026 Vp=0.7
```

3. Results

In this section, first the simulation results will be presented, followed by the experimental validation of the material integration approach.

3.1. Electronic simulation model

The previously introduced model was analyzed with respect to the conformance with experimental data and its suitability in circuit simulation. Fig. 3 shows the comparison of measured output curves with results from the simulated Verilog-A model. In the given V_{ds} range, the simplified mathematical and simulated model show good conformance with the experimental data. Fig. 3 (a) shows experimental data. It can be seen that due to process inaccuracies during fabrication or measurement setup, a spread in data between samples of different batches as well as slight variations within the same batch can appear. The data plotted in Fig. 3 (a) originate from physically different devices and different measuring runs (but with the same geometrical parameters). The points in the middle (vertical line) results from measurements of transfer characteristics measured with fixed V_{ds}=−0.3 V, whereas the other curves were measured with fixed V_{gs}. For both approaches, data for V_{gs}=0 V is presented. Fig. 3 (b) shows the mathematical model with G=2.6 × 10^{-3} S. The conductance can be derived from experimental data or by physical laws using physical and geometrical parameters (e.g., as proposed in [16]). Using experimental data, G can be derived by the slope of the mostly linear curve in the positive quadrant of the output characteristic or, less exactly, be approximated from the slope of the upper bound tangent line of the averaged curve in the negative quadrant of the output characteristic (see

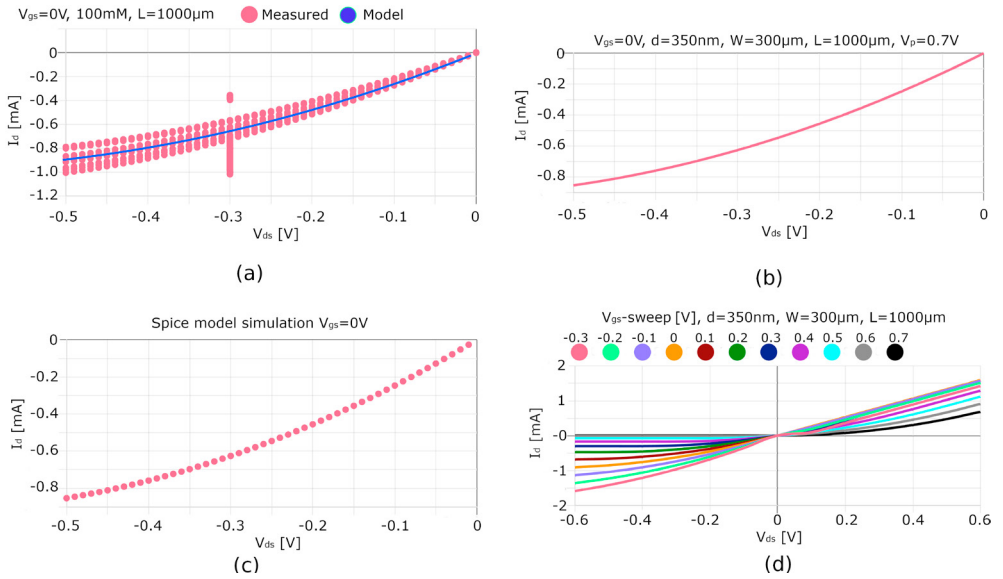


Fig. 3. Comparison of experimental output characteristics (at V_{gs}=0V) with the mathematical and the simulated Verilog-A models. (a) Measured (red) and simulated (blue) output curves (b) Mathematical model (c) Simulated Verilog-A model (d) Mathematical model curves for different gate voltages.

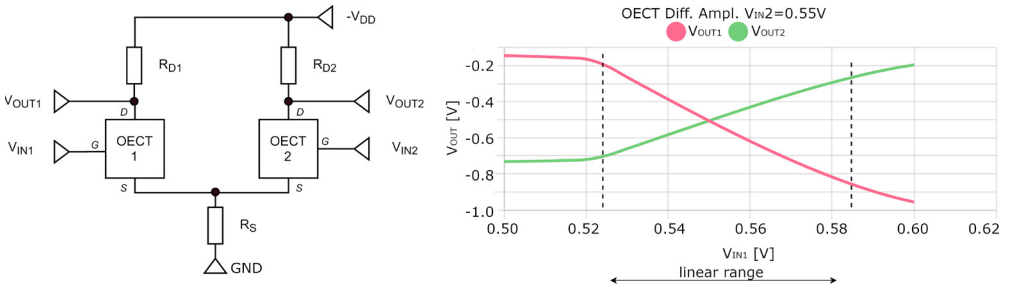
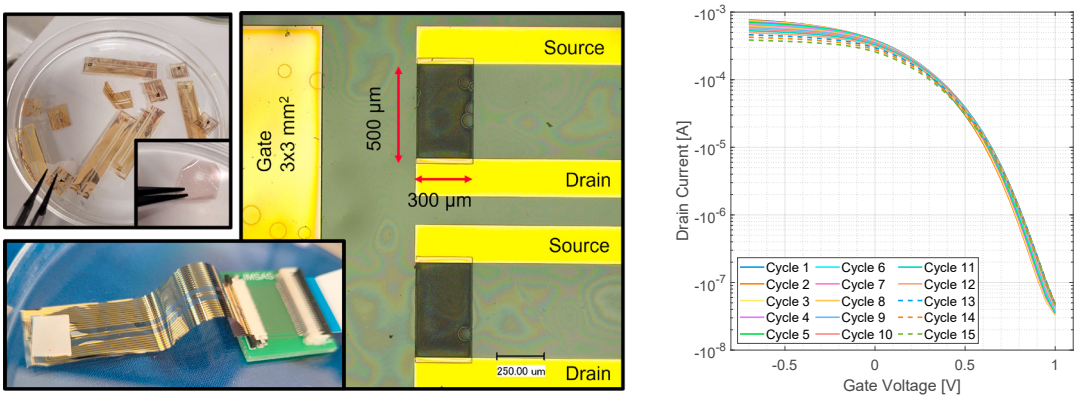


Fig. 4. (Left) OECT differential amplifier circuit (Right) V_{IN1}-V_{OUT} transfer diagram for V_{IN2}=0.55 V. The amplifier gain in the nearly linear range is about 10, with R_{S1}=10 kΩ, R_{D1}=R_{D2}=100 kΩ.

Fig. 3a). In this work G is approximated by the triangle spawned from the origin to the average I_d current at −0.3 V. The simulated data using the Verilog-A model and the mathematical model confirm exactly. There is also a good conformance of the simplified quadratic model with experimental data. Although, there are more physically correct models, e.g. presented in [17] considering a non-uniform ion mobility model, the used simplified quadratic model is well suited for electronic simulation, as shown in the next sub-section, without discontinuities and divergence behavior outside the proposed parameter range.

3.2. OECT Difference Amplifier

An OECT differential amplifier circuit (based on work in [6]) is shown in Fig. 4. The simulation was carried out with the simplified Verilog-A model presented in Def. 1. The results are pretty promising to compose more complex circuits such as operational amplifiers or artificial neural networks. The difference amplifier achieves a maximal gain of 10 with a non-linearity error below 10%.



(a) (b)

Fig. 5. a) Flexible OECTs for FRP integration. Top left: OECTs in water bath during lift-off, inset: separated sacrificial layer. Right: microscope image of channel structures. Bottom left: Device prepared for integration with solid electrolyte attached. b) Transfer curves varying due to increasing number of measurements.

3.3. Flexible OECTs under ambient conditions

Figure 5a shows the flexible OECTs during the lift-off step, immersed in DI water (top left), the sacrificial layer (top left inset), a microscope image of the achieved channel structures (right) and the OECT with attached solid electrolyte (bottom left), connected to the measurement interface. If no special precautions for increased stability are taken, a reduction in drain current on-off ratio, can be expected over multiple measurement cycles [4]. Similar effects are expected to be caused by increased temperatures. To be able to estimate by how much the drain current is reduced during repeated measurements and to which amount other factors during FRP plate manufacturing are responsible for this decay, multiple transfer curves were measured for one exemplary transistor under room conditions.

Fig. 5b shows the transfer characteristic of one representative transistor. It can be seen that there is a small but steady decrease of the on-current by 366 µA between the second and 15th measurement cycle. Also, an increase in the off-current over the course of the measurement cycles can be seen. However, this change is much smaller, it increases by 13.79 nA. It can be noted that the overall on-off ratio reduces slightly during these 15 cycles due to repeated measurements. Therefore, this change has to be considered when evaluating the effect of elevated temperatures in the next section.

3.4. Influence of elevated temperatures on flexible OECTs

For the following experiment, the OECTs were placed on top of a hotplate, covered by a perforated aluminum tray to limit heat flow while the temperature was stepwise increased from 30 °C to 130 °C and then held constant at 130 °C for 1 h. The results can be seen in Fig. 6a. For the first change in temperature, from 30 °C to 60 °C there is only a negligible change in the transfer behavior, however the off-current of is much higher than in the previous experiment. This might be caused by a shift in the threshold voltage. After reaching 130 °C, a reduced on current can be seen, accompanied by an off-current that is now in the expected range. The reduction in on-current corresponds to 164 µA from 30 °C to 60 °C, larger than due to repeated measurements. It can also be seen that the whole transfer curve shifts to lower gate voltages so that a clearly defined off- or rather minimum current of −151 nA can be seen. Leaving the sample at elevated temperatures for 1 h without measuring in between even shows a more drastic effect. The on-current further reduces by 454 µA to −118 µA, while the minimum current increases by 147 nA to −298 nA. This trend continues with continuous measurements started after waiting at 130 °C for 1 h. The on-current steadily reduces but the off current reduces again slightly until the shift saturates around −23 nA for the last measurement cycles.

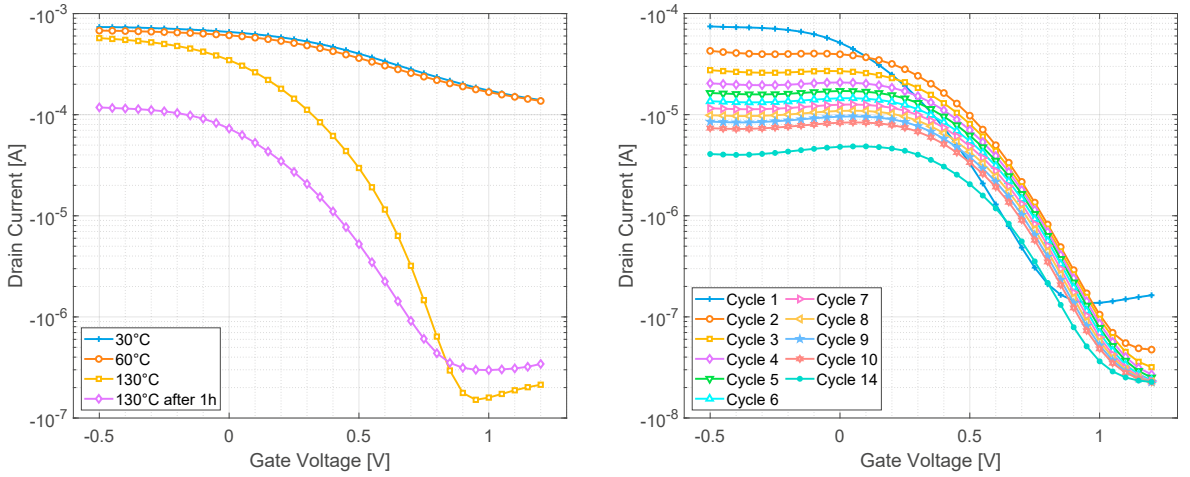


Fig. 6. Transfer curves of flexible OECTs during increased temperatures on a hotplate. a) During heat-up and after holding 130°C for 1 h. b) During multiple measurements at 130°C.

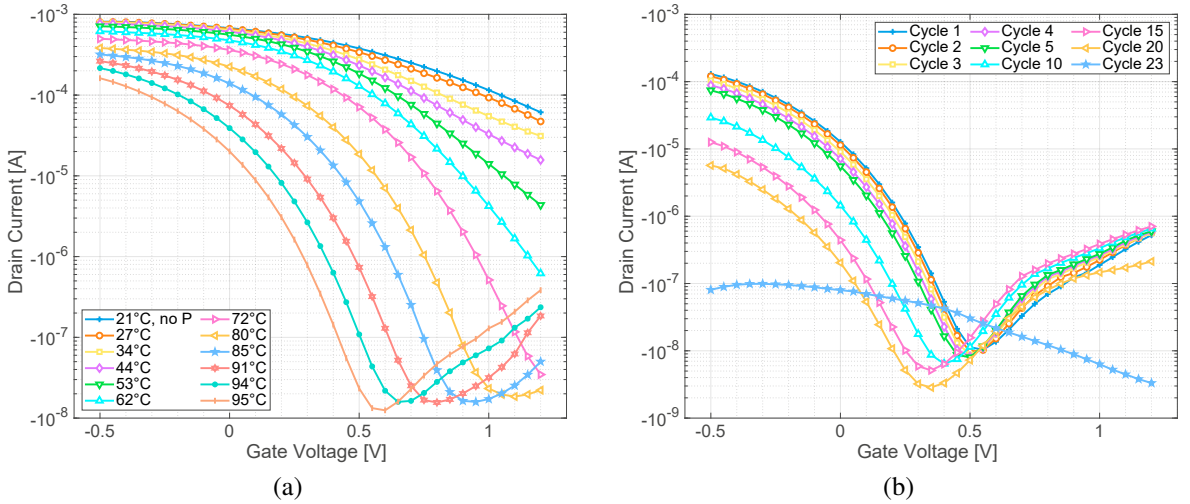


Fig. 7. Transfer curves of flexible OECTs during the embedding process into FRP. a) During heat-up ramp, measurements recorded every 5 min, average temperatures during measurement duration in legend. b) During hold phase, T=const., recorded every 4.5 min.

3.5. Influence of the embedding process on flexible OECTs

For the final experiment, three samples, containing 10 OECTs each, were embedded into FRP plates using the process described in Sec. 2.3. Three samples were prepared. Two of which were left exposed to the resin flow, while one sample was covered using Polyimide Film Electrical Tape 92 with Silicone Adhesive (3M, Austin, Texas, USA). Two transistors on one of the exposed samples were continuously measured during the embedding process to compare the influence during embedding to the experiment presented before, only experiencing heat exposure on the hotplate. During heat-up, measurements were taken every five minutes, while the start and end temperatures over this time frame were recorded as reference.

The results of one transistor are presented in Fig. 7a, the second transistor showed exactly the same behavior. The first measurement was performed after preparing the setup, already under vacuum but without any external pressure or temperature, represented by the blue curve, '+' marker. The measurement with external pressure applied but still at room temperature is represented by the orange curve, 'o' marker. There is only a slight difference between these two

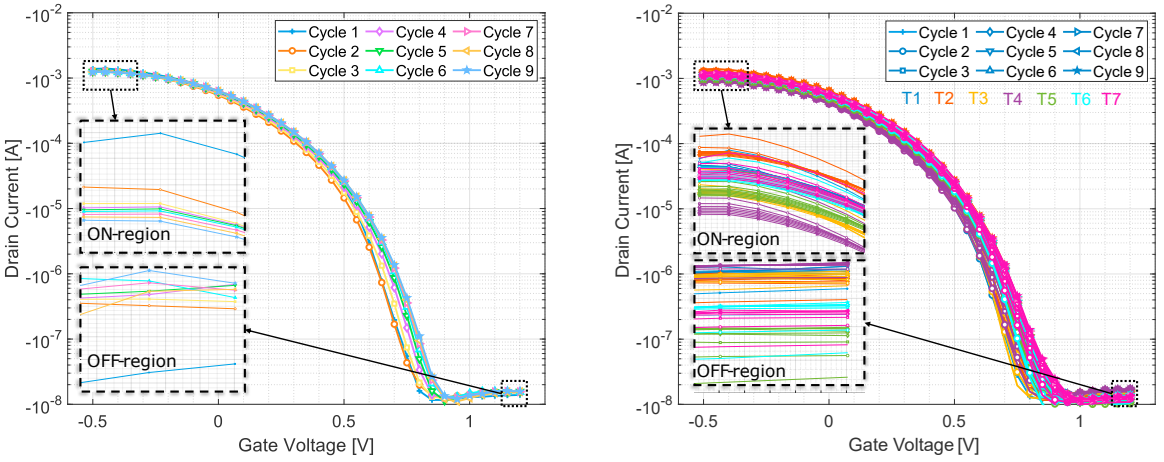


Fig. 8. Transfer curves after embedding into FRP plates, change over 9 measurement cycles. a) For a single transistor. b) For seven different transistors on the same substrate.

curves, which perfectly aligns with the trend caused by increasing temperatures visible in the other curves, leading to the conclusion that the externally applied pressure of the hotpress does not affect the transfer behavior of the OECTs noticeably.

With increasing temperatures, a similar effect as already seen in the previous experiment can be seen. The transfer curves shift to lower gate voltages while the on-current reduces. This reduction is higher than that of the repeated measurements presented in Figure 5, leading to the assumption that this is induced by increasing temperature. Also, an atypical increase at high positive gate voltages after reaching a minimum current can be observed.

During the hold time of the hot-press at 95 °C, measurements are taken continuously (i.e. ≈ 4.5 min per measurement cycle) until the end of the embedding process, presented in Fig. 7b. It can be seen that the transfer curves are shifted with every measurement to lower gate voltages, while the on-current reduces steadily with every measurement. From cycle 23 onward, the device shows no typical transfer behavior anymore, the transistor is broken.

3.6. Successful integration of OECTs into FRP

After completing the embedding procedure, none of the uncovered samples survived the embedding process unharmed. The OECTs on these samples showed a noteworthy increased channel resistance and basically no current modulation after the process.

To avoid this degradation of the OECT during embedding, two adjustments of the process can be taken. First of all, the samples are encapsulated by covering them with tape before the process. Furthermore, the samples are not continuously measured at elevated temperatures to reduce the applied electrical and temperature stress.

The result is shown in Figure 8a. It can be seen that the transfer curves are very stable, actually much more stable than those measured in ambient conditions shown in Figure 5. A small shift in the curves can be noticed but the on- and off-current are highly stable over multiple cycles. Figure 8b shows 9 forward cycles of the transfer curves for seven different OECTs on the same substrate and inside the same FRP sample after the embedding process. It can be seen that the devices are not only consistently very stable over multiple measurement cycles (marked by different symbols), but also deviate only slightly between the different transistors (marked by different line colors).

However, at this point it has to be noted that all seven transistors are on the same substrate, embedded into the same piece of FRP. Therefore for different OECT fabrication batches and different embedding processes, variations are expected within a certain range. Identifying the spread in OECT characteristics over a larger amount of specimens will be required in upcoming work to finetune both, simulation models and the embedding process alike.

4. Conclusion and outlook

Adding processing capabilities to sensors embedded in hybrid materials will lead to increased performance and higher acceptance of SHM systems. A simplified OECT Verilog-A model directly derived from a mathematical model was compared with experimental data. Although, basically a quadratic function $I_d(V_{gs},V_{ds})$ was assumed, the transfer curves showed a suitable conformance with experimental data in the third quadrant, the most important one for p-type depletion OECT operation, including the saturation range of the device. There were no difference observed between the mathematical model and the output of the electronic simulation using *ngspice* and the Verilog-A model. A simple single-stage difference amplifier using two OECT devices and three resistors was simulated using this model. The linearity of the transfer curve of the amplifier is acceptable for approximated analog computing with a suitable amplifier gain of 10. The electronic model can be parameterized by the geometrics of the channel or by providing experimental parameters. As a first step into the direction of implementing such circuits, we successfully integration OECTs into FRP plates, yielding transistors with even higher cyclic stability inside the material compared to devices characterized in ambient conditions. The key to successfully embedding OECTs into FRP could be found in encapsulating the device and not performing any measurements during the embedding process. In the future the simulation model should be refined and should include environmental parameters like temperature or mechanical stress, basically derived from experimental data of real devices under various environmental conditions.

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Appendix A. Simulation model

Ex. 1. Spice simulation circuit for the difference amplifier using the Verilog-A transformed model from Def. 1

```
.model oect oect G=0.0026 Vp=0.7

V1  VSS 0 -1
VIN  VG1 0 0
VREF VG2 0 0.55

* G D S
NMN1 VG1 OUT1 SG oect
NMN2 VG2 OUT2 SG oect
RS1  SG 0 10000
RD2  OUT1 VSS 100000
RD3  OUT2 VSS 100000

.control
  * load the model dynamically
  pre_osdi ./oect.osdi
  dc VIN 0.5 0.6 0.005
  print V(VG1) V(VG2) V(OUT1) V(OUT2)
  set filetype = ascii
  write output.dat V(VG1) V(VG2) V(OUT1) V(OUT2)
.endc
.end
```