Integration of Organic-Electrochemical Transistors into Composite Material for Structural Health Monitoring

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Abstract: Monitoring the structural health of composite materials such as fiber-laminates is essential for the safe use of these materials e.g. in the aviation or building sector. Thin and flexible sensors as well as signal processing circuits based on organic-electrochemical transistors (OECTs) can potentially be embedded into composite materials, providing a means of sensing and data processing inside the material of monitoring for potential damage. In the current work, OECTs are investigated for their potential to be integrated into composite panels. Specifically, we investigate the stability of OECTs inside fiber laminates and the influence of processing conditions (temperature, pressure) on the device performance. During processing of composite plates, the devices will be exposed to high temperatures and high pressures, which can lead to a change in the properties of the OECTs, potentially damaging the devices. Besides investigating the integration and technological issues, simulation of OECT devices using Verilog-A models and the Spice3 simulator as well as a composition of a small signal processing circuit should be studied. The parameterizable simulation model should be adapted to experimental OECT characteristic curves. We will outline the roadmap to fully integrated smart sensors and sensor networks using additive technologies and in-sensor analog signal and information processing. The goal is to integrate the entire information and communication technology in analog electronics providing advantages in power consumption and component density compared to digital and microcontroller circuits commonly used in sensor nodes. We investigate the behavior of real devices as well as electronic simulation using Verilog-A device models based on physical models and experimental data. A simple OECT difference amplifier circuit is analyzed.

1. Introduction

In order to investigate the suitability of implementing such material-integrated data processing using OECTs, the effects of the embedding process are investigated in detail. For this, the OECTs are exposed to high temperatures separately before they are finally integrated into the material, while changes in the OECT transfer behavior are evaluated. The aim of this study is to determine the challenges and limits of OECT material integration for monitoring purposes, as well as to identify the most important areas for improvement to successfully use OECTs for this purpose in the future.
Additionally, the electronic modeling required for circuit development is investigated. The aim is a parameterizable Verilog-A model that can be used for circuit simulation, e.g., by using the *ngspice* simulator software [3]. This model should provide the following features:

1. Transfer characteristics close to real components (small reality gap);
2. Transfer characteristics based on geometrical and physical parameters, e.g., channel width;
3. Inclusion of environmental parameters, e.g., temperature, strain, pressure;

4. History, i.e., a state-base model (not considered in this work), because the experimental study in this work shows hysteresis and altering effects.

In this work we investigate preliminary simplified models, actually not covering environmental parameters like temperature or mechanical stress and there impact on the device behavior and transfer curves. But we show the principles to derive a simulation model and its constraints, finally used in an electronic simulation of a single-stage OECT difference amplifier.

2. Electronic Simulation and Electronic Modeling

There are different models available for the electronic modeling of OECT devices. They differ in physical accuracy and parameterization, e.g. a quadratic-law model [1] versa a power-law model in [4]. Such models can be classified in:

1. Physical models used for the description and evaluation of the transfer characteristics and deeper understanding of ion flows;
2. Surrogate models that are used in electronic simulation for circuit design and test.

The first model class uses such models commonly in specific parameter ranges including input and output currents and voltages, i.e., in the interpolation range, whereas the second model class is used by a electrical circuit solver or, e.g., by a Machine Learning trainer supporting analog Artificial Neural Networks. The second use-case cannot guarantee that the model is used in its intended parameter space, interpolation as well extrapolation can occur, which can be have a significant impact on the use-case. We have two design goals for these models:

1. Accuracy and precision with respect to real devices;
2. "Smooth" model behavior in the extrapolation space, i.e., avoiding steep gradients, divergence, or oscillation outside of the intended parameter space (e.g., input current).

This work investigates primarily the impact of device integration into materials on the device characteristics and transfer curves. Therefore, the physical as well electronic models have to be sensitive and parameterizable to environmental parameters, at least the temperature. In contrast to temperature effects, which can be easily modeled, mechanical effects are hard to be modeled. The electronic model introduced in the next sub-section will actually not consider environmental effects and should be considered as a starting point for electronic simulation.

2.1 Electronic Model

The electronic model describes the drain current I_d in dependence of the drain-source voltage V_ds and the gate-source voltage V_gs and bases on a simplified ion mobility model from [1], basically a quadratic function. The mathematical model is split in different quadrants depending on the polarity of V_ds and the relation of V_gs to V_ds or V_dsat, which is the difference of V_gs and the pinch-off voltage V_p:

$$V_{dsat} = V_{gs} - V_p$$

$$I_d = \begin{cases} \begin{cases} G \cdot \left(1 - \frac{V_{gs} - 0.5 \cdot V_{ds}}{V_p}\right) \cdot V_{ds} & , \quad V_{ds} \leq V_{gs} \\ G \cdot \left(V_{ds} - \frac{V_{gs}^2}{2 \cdot V_p}\right) & , \quad V_{ds} > V_{gs} \end{cases} & , \quad V_{ds} > 0 \\ \begin{cases} -\frac{G \cdot V_{dsat} \cdot V_{dsat}}{2 \cdot V_p} & , \quad V_{ds} \leq V_{dsat} \\ G \cdot \left(1 - \frac{V_{gs} - 0.5 \cdot V_{ds}}{V_p}\right) \cdot V_{ds} & , \quad V_{ds} > V_{dsat} \end{cases} & , \quad V_{ds} \leq 0 \end{cases} \tag{1}$$

The functional-equivalent Verilog-A model is shown in Def. 1. The model is converted into an OSDI model using the *openvaf* tool, which can be finally imported by *ngspice*. The model can be parameterized by the channel conductance *G* and pinch-off voltage *Vp* to fit the model to real devices.

Def. 1. Simple four-quadrant quadratic Verilog-A OECT $I_D(V_{GS},V_{DS})$ model using experimentally measured conductance G and pinch-off voltage V_p parameters.

```
1: module oect(g,d,s);
2: inout g,d,s;
3: electrical g,d,s;
4: parameter real G=2e-3;      // The Channel Conductivity (S)
5: parameter real Vp=0.65;     // Pinch-off voltage (V)
6: real Vgs,Vds,Vdsat,Ids;
7: analog begin
8:   Vgs=V(g,s);
9:   Vds=V(d,s);
10:  Vdsat=Vgs-Vp;
11:  //REGION CURRENTS//
12:  if (Vds > 0) begin
13:    if (Vds<=Vgs) begin
14:      Ids=G*(1-(Vgs-0.5*Vds)/Vp)*Vds;
15:    end else begin
16:      Ids=G*(Vds-pow(Vgs,2)/(2*Vp));
17:    end
18:  end else begin
19:    if (Vds<=Vdsat) begin
20:      Ids=-(G*Vdsat*Vdsat)/(2*Vp);
21:    end else begin
22:      Ids=G*(1-(Vgs-0.5*Vds)/Vp)*Vds;
23:    end
24:  end
25:  I(d,s)<+Ids;
26: end
27: endmodule
28: // model usage in SPICE
29: .model oect oect G=0.002 Vp=0.7
```

2.2 Results

The previously introduced model was analyzed with respect to the conformance with real measured data and its suitability in circuit simulation. Fig. 1 shows the comparison of real measured I_D-V_{DS} transfer characteristics with results from the simulated Verilog-A model. In the given V_{DS} range the simplified mathematical and simulated model show good conformance with the measured data. Fig. 1 (a) shows measured data. As discussed in this paper, the devices show variance. The data plotted in Fig. 1 (a) originate from physically different devices and different measuring runs (but with same geometrical parameters). The measuring points in the middle (vertical line) results from measurements with fixed V_{ds} voltage, whereas the other curves were measured with fixed V_{gs} voltage, Fig. 1 (b) shows the mathematical model with measured conductance G=2.6 10^{-3}S. The measured conductance G can be derived approximately from the slope of the upper bound tangent line of the averaged curve in the negative quadrant of V_{ds}-I_d (see Fig. 1a), in this work approximated by the triangle spawned from the origin to the average

I_d current at -0.3V, or more exactly by the slope of the mostly linear curve in the positive quadrant of V_{ds}-I_d. The simulated data using the Verilog-A model and the mathematical model confirm exactly. There is a good conformance of the simplified quadratic model with experimental data. The conductance G can be derived from experimental data or by physical laws using physical and geometrical parameters (e.g., as proposed in [5]). Although, there are more physically correct models, e.g. presented in [4] considering a non-uniform ion mobility model, the used simplified quadratic model is well suited for electronic simulation, as shown in the next sub-section, without discontinuities and divergence behavior outside the proposed parameter range.

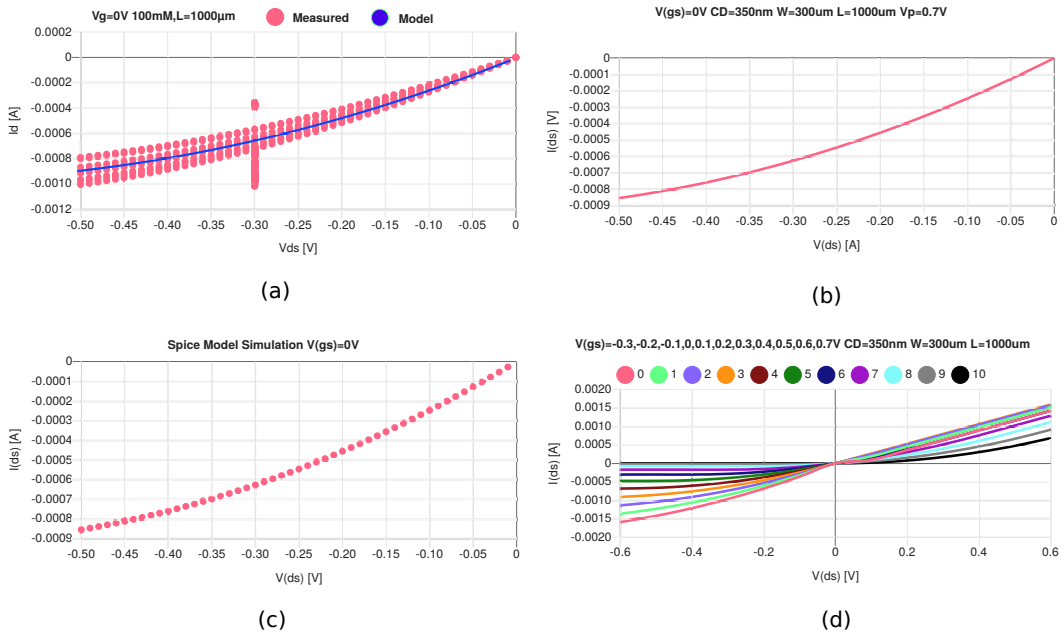

Fig. 1. Comparison of real measured I_D-V_{DS} transfer characteristics (at V(GS)=0) with the mathematical and the simulated Verilog-A models. (a) Measured transfer curve and simulated curve (b) Mathematical model (c) Simulated Verilog-A model (d) Mathematical model curves for different gate voltages

2.3 OECT Difference Amplifier

An OECT differential amplifier circuit (based on work in [2]) is shown in Fig. 2. The simulation was carried out with simplified Verilog-A model defined in Def. 1. The results are pretty promising to compose more complex circuits such as operational amplifiers or artificial neural networks. The difference amplifier achieves a maximal gain of 10 with a non-linearity error below 10%.

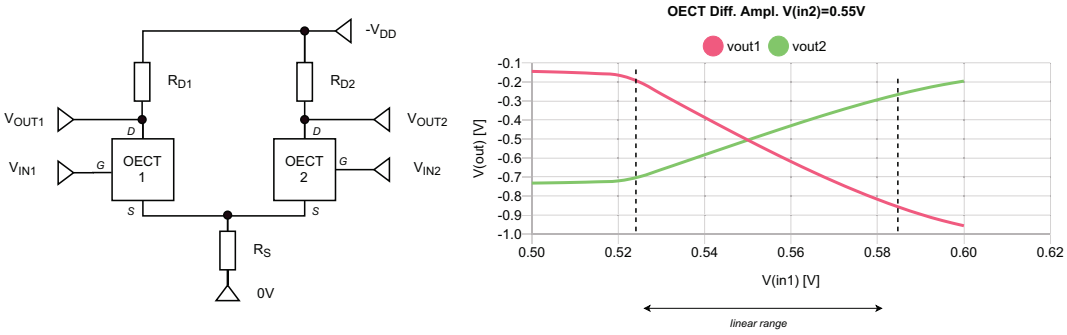

Fig. 2. (Left) OECT differential amplifier circuit (Right) V_{IN1}-V_{OUT} transfer diagram for V_{IN2}=0.55V. The amplifier gain in the nearly linear range is about 10, with R_{S1}=10kΩ, R_{D1}=R_{D2}=100kΩ

3. Conclusions

A simplified OECT Verilog-A model directly derived from a mathematical model was compared with experimental data. Although, basically a quadratic function $I_d(V_{gs}, V_{ds})$ was assumed, the transfer curves showed a good conformance with experimental data in all four quadrants including the saturation range of the device. There were no difference observed between the mathematical model and the output of the electronic simulation using *ngspice* and the Verilog-A model. A simple single-stage difference amplifier using two OECT devices and three resistors was simulated using this model. The linearity of the transfer curve of the amplifier is acceptable for approximated analog computing with a suitable amplifier gain of 10. The electronic model can be parameterized by the geometrics of the channel or by providing experimental parameters. The molarity of the electrolyte is actually not included.
In the future the model should be refined and should include environmental parameters like temperature or mechanical stress, basically derived from experimental data of real devices under various environmental conditions.

4. Appendix

Ex. 1. Spice simulation circuit for the difference amplifier using the Verilog-A transformed model from Def. 1

```
1: .model oect oect G=0.0026 Vp=0.7
2:
3: V1  VSS 0 -1
4: VIN  VG1 0 0
5: VREF VG2 0 0.55
6:
7: * G D S
8: NMN1 VG1 OUT1 SG oect
9: NMN2 VG2 OUT2 SG oect
10: RS1  SG 0 10000
11: RD2  OUT1 VSS 100000
12: RD3  OUT2 VSS 100000
```

```
13:
14: .control
15:   * load the model dynamically
16:   pre_osdi ./oect.osdi
17:   dc VIN 0.5 0.6 0.005
18:   print V(VG1) V(VG2) V(OUT1) V(OUT2)
19:   set filetype = ascii
20:   write output.dat V(VG1) V(VG2) V(OUT1) V(OUT2)
21: .endc
22: .end
```

5. References

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[3] Vogt, H., Hendrix, M., Nenzi, P., & Warning, D. (2021). Ngspice User's Manual Version 36 (ngspice release version). URL: http://ngspice. sourceforge. net/docs/ngspice-35-manual. pdf (visited on 2022-08-24)

[4] P. Sideris, S.Siskos, and G. Malliaras, Verilog-A Modeling of Organic Electrochemical Transistors, in 2017 6th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2017

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